a group of individual instructions to be executed in parallel to an appropriate processing pipeline, the method comprising:

retrieving a very long instruction word from a main memory;

storing in a very long instruction word storage **[an instruction frame]** the very long instruction word retrieved from the main memory, the **[frame]** very long instruction word including **[at least one group]** groups of individual instructions to be executed in parallel, each individual instruction in **[the]** a group of individual instructions having **[associated therewith]** embedded therein a pipeline identifier indicative of **[the]** a processing pipeline which will execute that individual instruction and having embedded therein a group identifier indicative of **[the]** a group identification;

comparing **[the]** a group identifier **[of]** for each individual instruction in the **[instruction frame]** very long instruction word with an execution group identifier of those instructions to be next executed in parallel; and

using **[the]** a pipeline identifier **[of]** for those instructions to be next executed in parallel to control switches in a crossbar switch having a first set of connectors coupled to the very long instruction word storage for receiving **[instructions]** the very long instruction word therefrom and a second set of connectors coupled to the plurality of processing pipelines to thereby supply each individual instruction in the at least one group to be executed in parallel to the appropriate processing pipeline.

REMARKS

Claims 1-23 were pending. Upon entry of the present preliminary amendment, amending claims 1-23, claims 1-23 will be pending.

The Claimed Invention

The claimed invention relates to a computer architecture, and in particular to an architecture in which groups of instructions may be executed in parallel, as well as to methods and apparatus for accomplishing the same.

Previously Cited Art

Iizuka:

Iizuka relates to a parallel processing device which processes plural instructions in parallel. Iizuka discloses:

> The prior very long instruction word (VLIW) parallel computer required a data bus having a width of 128 bits in order to execute four basic instructions as a single word per clock cycle, but according to the configurations explained above, a parallel computer such as each of the above embodiments requires an instruction bus and a data bus having a width of only 32 bits in order to perform equivalently while maintaining the same high speed information processing capacity as the prior parallel computer. (Emphasis added). Col. 10, lines 41-49.

In light of the stated purpose, Iizuka discloses:

> [A] multiple-port expanded instruction register which selectively stores the computer instructions in its entries and causes the instructions in the entries to be executed simultaneously, or two-dimensional expanded instruction register which sequentially stores the computer instructions in its two dimensional entries specified by the line and column and causes plural computer instructions to be simultaneously executed by specifying the specific line. (Emphasis added). Col. 10, line 65 - Col. 11, line 5.

Iizuka describes, in order to parallel process instructions:

> [I]nstruction decoder 105 decodes [the contents of external memory 122], specifies thereby a line and a column according to the information of the destination operand of decode instruction 121 in instruction register 147, specifying thereby one of the entries in two-dimensional expanded instruction register 148, and stores the decoded result (micro instruction) in the specified entry. (Emphasis added). Col. 7, lines 43-49.

Iizuka continues:

> This operation is repeated to store the micro instruction in each entry corresponding to each of the processing pipelines 112 to 115. (Emphasis added). Col. 7, lines 50-52.

Importantly, Iizuka also describes:

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> [An] equivalent of four instructions per clock cycle is continued to be executed as long as parallel execute instruction 131 is repeated. (Emphasis added). Col. 8, lines 11-14.

What Iizuka in effect appears to disclose is a serial-in, parallel-out two-dimensional register, that operates at run-time, containing instruction words.

Morrison et al.:

Morrison et al. relates to a parallel processor computer system having software for detecting natural occurrences in instruction streams and having a plurality of processor elements for processing the detected natural concurrences.

Morrison et al.'s TOLL software:

> [E]xamines each individual instruction and its resource usage both as to type and as to location ... then assigns instruction firing times (IFTs) [and] .. reorders the instruction stream based upon these firing times (e.g., Table 5). Col. 13, lines 44-49. (Emphasis added.)

Morrison et al.'s hardware includes an instruction portion 1510:

> One purpose of the instruction portion 1510 [in Fig. 15] is to receive execution sets from memory, place the sets into the caches 1522 and furnish the instructions within the sets, on an as needed basis, to the processor elements 640. Col. 30, lines 25-29.

In operation:

> The instruction caches selection portion 1510 receives the instructions of an execution set from the memory bus 1524 and, in a round robin manner, places instructions word into each cache partitions, 1522a, 1522b, 1522c and 1522d. Col 30, lines 53-57. (Emphasis added.)

What Morrison et al. in effect appears to disclose is hardware and software supporting a serial-in, parallel-out cache, that operates at run-time, containing instruction words.

The Claimed Invention

The claimed invention relates to a computer architecture incorporating superscaler and very long instruction word concepts.

Claim 1 as amended recites, among other elements, a main memory for storing a very long instruction word. Claim 1 also recites a very long instruction word storage, coupled to the main memory, for receiving the very long instruction word from the main memory, and for holding the very long instruction word, the very long instruction word including a predetermined number N of individual instructions, and including at least one group of M individual instructions to be executed in parallel, where $M \leq N$, each individual instruction in the very long instruction word storage to be executed having a pipeline identifier indicative of a processing pipeline for executing the individual instruction, and having a group identifier indicative of a group of individual instructions to which the individual instruction is assigned for execution in parallel.

Claim 6 as amended recites, among other steps, forming a very long instruction word with a fixed number of the instructions including at least the group of instructions having the common group identifier as well as at least one other instruction having a different group identifier. Claim 6 also recites storing the very long instruction word in a main memory.

Previously Cited Art Distinguished

Neither Iizuka nor Morrison et al. disclose the presently claimed invention for the reasons set forth below.

Claim 1 recites, among other elements, a main memory for storing a very long instruction word, neither Iizuka nor Morrison et al. disclose this limitation.

Iizuka appears to disclose a computer architecture that specifically avoids storing very long instruction words. In contrast to claim 1, Iizuka specifically describes the object of its invention is to provide a parallel processing device using ordinary bit width buses.

Morrison et al appears to disclose a computer architecture that also specifically avoids storing very long instruction words. In contrast to claim 1, Morrison et al.

specifically describes that streams of instructions are generated and the instructions in the streams are re-ordered based upon firing times, i.e. the instructions are stored individually.

Claim 1 also recites a very long instruction word storage, coupled to the main memory, for receiving the very long instruction word from the main memory, and for holding the very long instruction word, the very long instruction word including a predetermined number N of individual instructions, and including at least one group of M individual instructions to be executed in parallel, where $M \leq N$, each individual instruction in the very long instruction word storage to be executed having a pipeline identifier indicative of a processing pipeline for executing the individual instruction, and having a group identifier indicative of a group of individual instructions to which the individual instruction is assigned for execution in parallel, Iizuka and Morrison et al. do not disclose this limitation.

Iizuka appears to disclose a computer architecture that only includes a single group of instructions to be executed in parallel. In contrast to claim 1, Iizuka specifically describes a two-dimensional instruction register which receives and sequentially stores individual instructions and causes the instructions to be executed simultaneously by specifying the specific line of instructions in the register to be executed.

Morrison et al. appears to disclose a computer architecture that only includes individual caches for holding instructions to be executed in parallel. In contrast to claim 1, Morrison specifically describes individual caches for receiving individual instructions one by one and storing the instructions to be executed in separate cache locations.

Claim 6 recites, among other steps, forming a very long instruction word with a fixed number of the instructions including at least the group of instructions having the common group identifier as well as at least one other instruction having a different group identifier, Iizuka does not disclose this limitation.

Iizuka appears to disclose a computer architecture that only includes a single group of instructions to be executed in parallel. In contrast to claim 6, Iizuka specifically describes only storing individual instructions to be executed simultaneously in a line in a two-dimensional register.

Claim 6 also recites storing the very long instruction word in a main memory. neither Iizuka nor Morrison et al. disclose this.

Iizuka appears to disclose a computer architecture that specifically avoids storing very long instruction words. In contrast to claim 6, Iizuka specifically describes only storing ordinary bit width instructions.

Morrison et al. appears to disclose a computer architecture that also specifically avoids storing very long instruction words. In contrast to claim 6, Morrison et al. specifically generates serial streams of instructions and only stores the instructions as a serial stream of instructions.

Because neither Iizuka nor Morrison et al. disclose, among other elements, a main memory for storing a very long instruction word, nor a very long instruction word storage, coupled to the main memory, for receiving the very long instruction word from the main memory, and for holding the very long instruction word, the very long instruction word including a predetermined number N of individual instructions, and including at least one group of M individual instructions to be executed in parallel, where $M \leq N$, each individual instruction in the very long instruction word storage to be executed having a pipeline identifier indicative of a processing pipeline for executing the individual instruction, and having a group identifier indicative of a group of individual instructions to which the individual instruction is assigned for execution in parallel, as claimed in claim 1, claim 1 is allowable. Claims 2-5, dependent upon allowable claim 1, are also allowable.

Independent claims 11 and 16 are also allowable for substantially the same reasons as claim 1. Claims 12-15 and 17-19, respectively dependent upon allowable claims 11 and 16, are also allowable.

Because neither Iizuka nor Morrison et al. disclose, among other steps, steps, forming a very long instruction word with a fixed number of the instructions including at least the group of instructions having the common group identifier as well as at least one other instruction having a different group identifier, nor storing the very long instruction word in a main memory, as claimed in claim 6, claim 6 is allowable. Claims 7-9, dependent upon allowable claim 6, are also allowable.

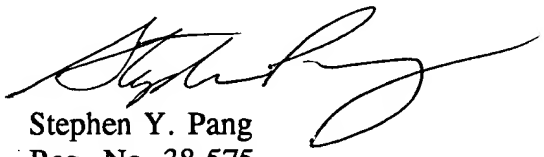
Independent claims 10, 20, and 23 are also allowable for substantially the same reasons as claim 6. Claims 21-22, dependent upon allowable claim 20, are also allowable.

Conclusion

Consideration of this application as amended is respectfully requested. Allowance of all pending claims is earnestly solicited.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (415) 326-2400.

Respectfully submitted,



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